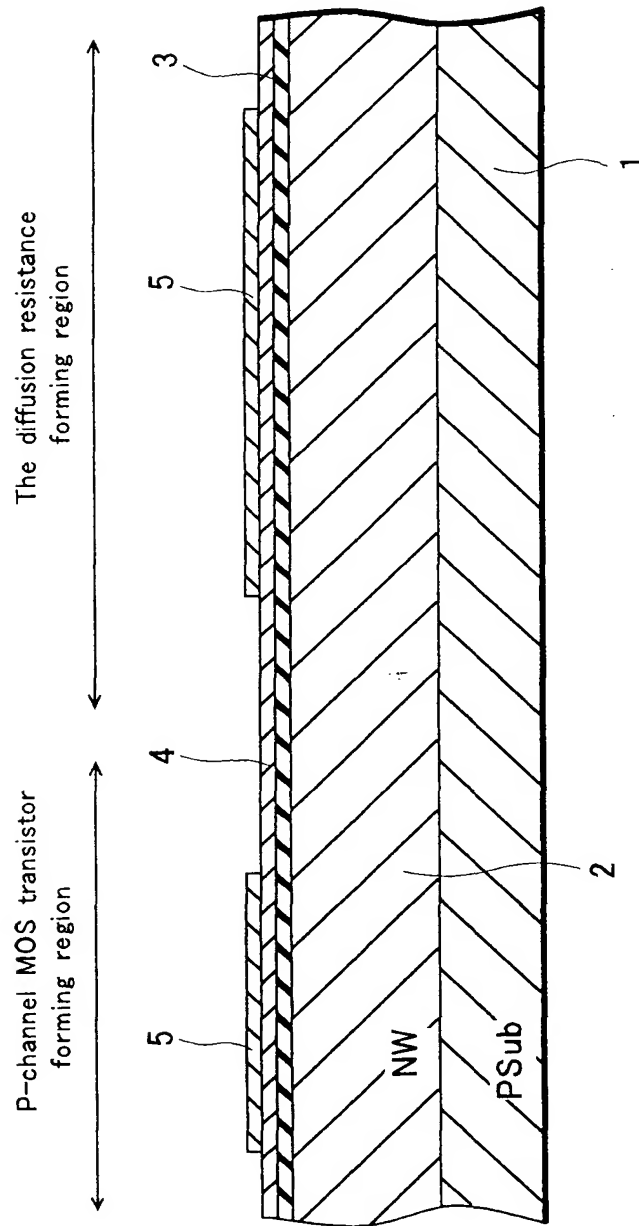


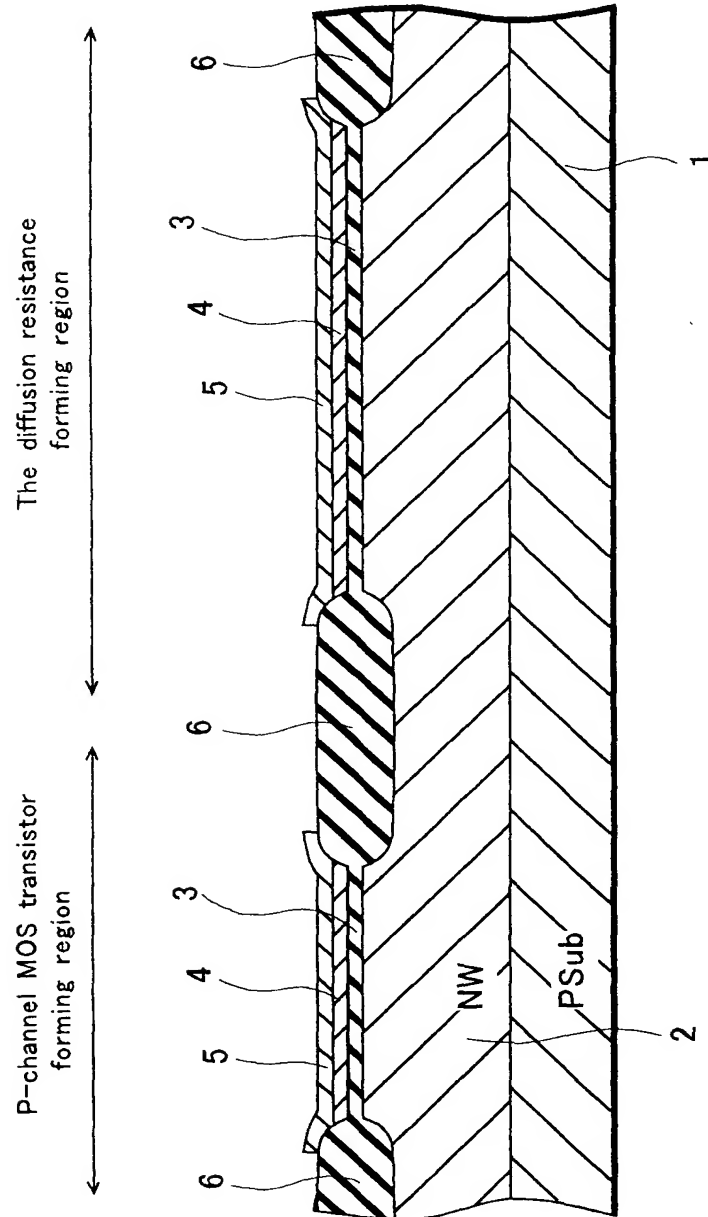
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FIG. 1



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FIG.2



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FIG.3

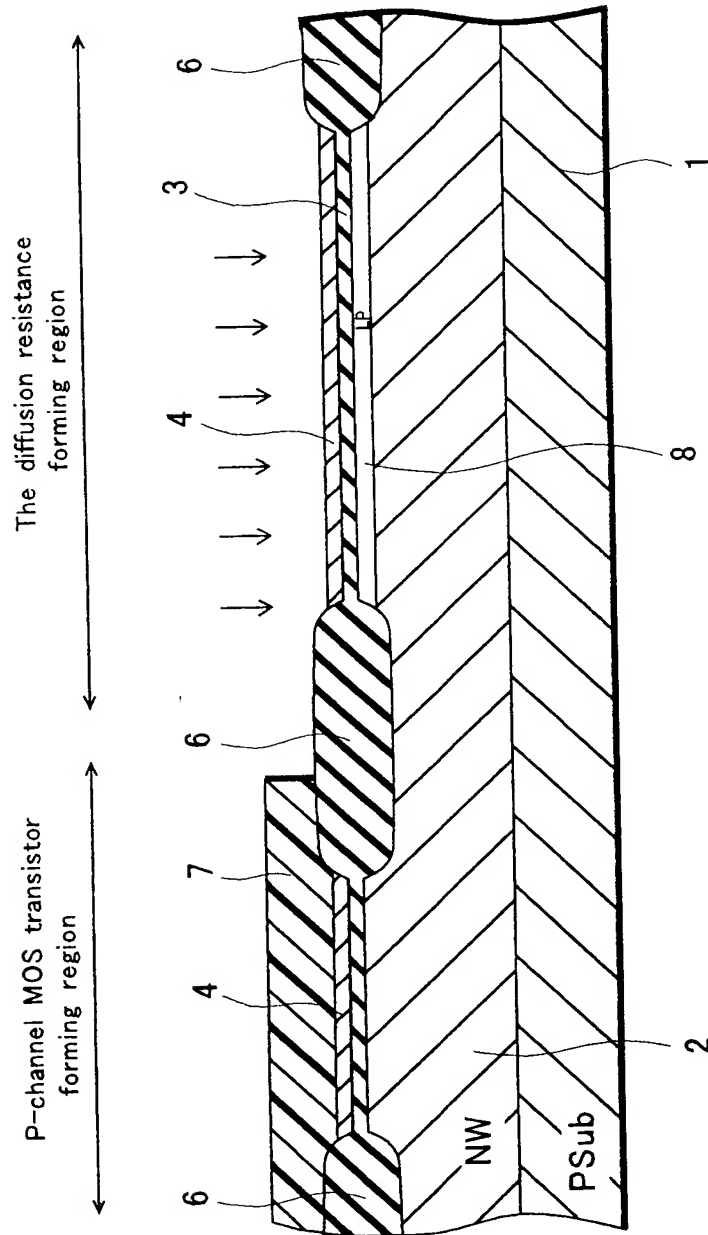
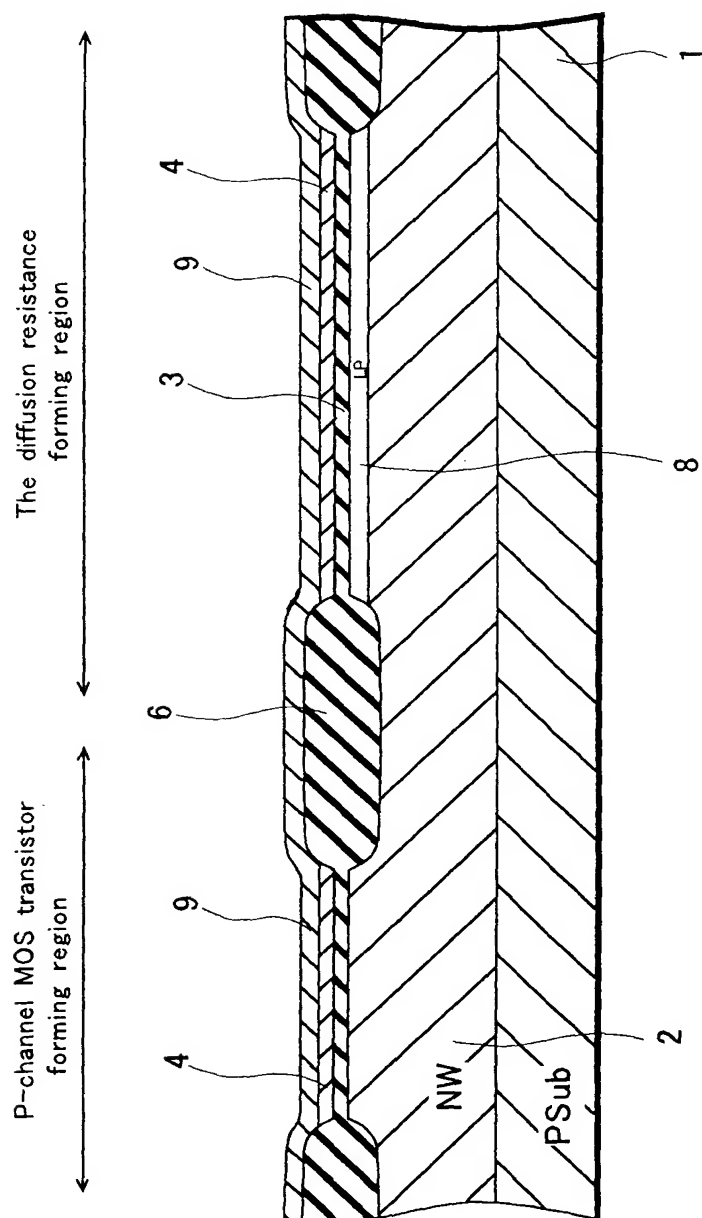


FIG.4



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FIG.5

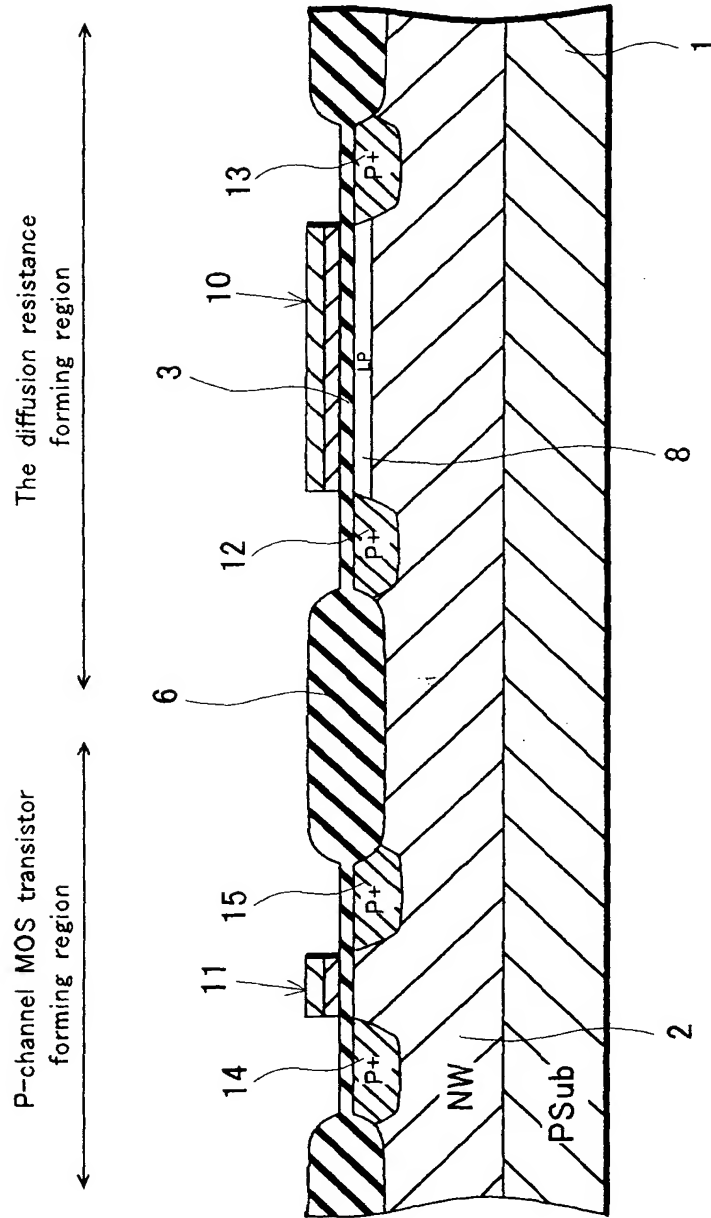


FIG.6

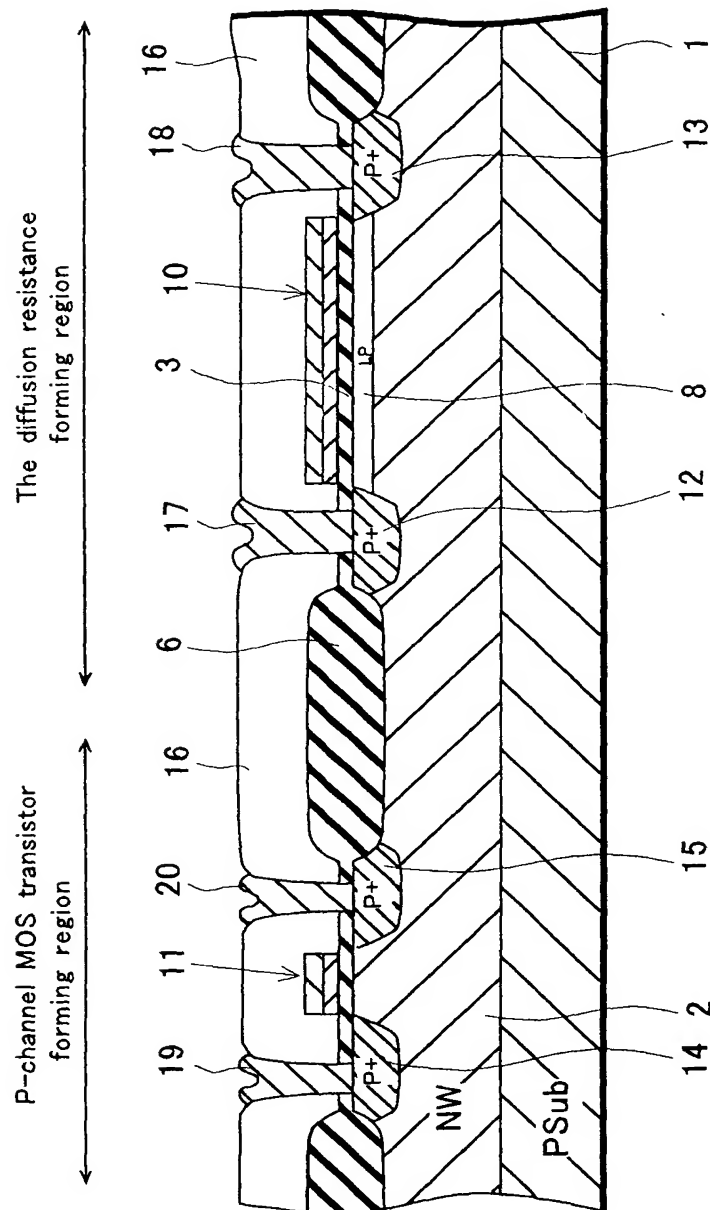


FIG.7

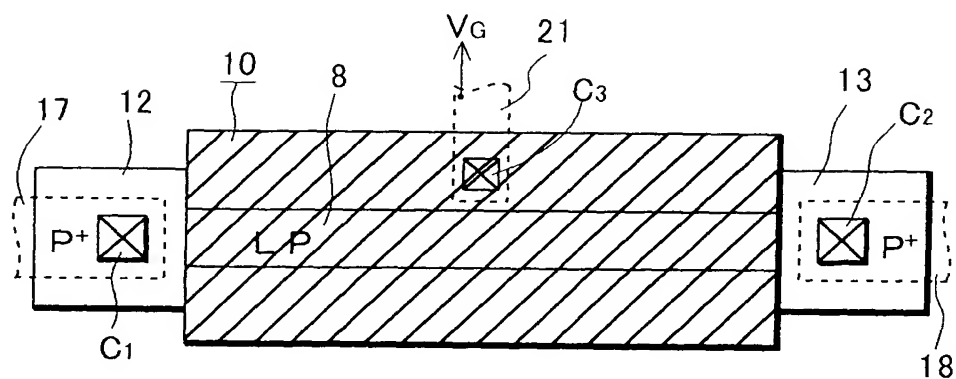
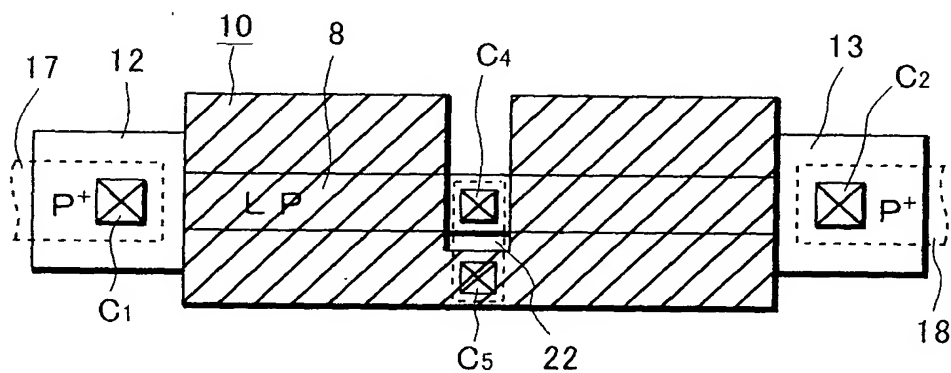


FIG.8



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FIG.9(A)

R=0

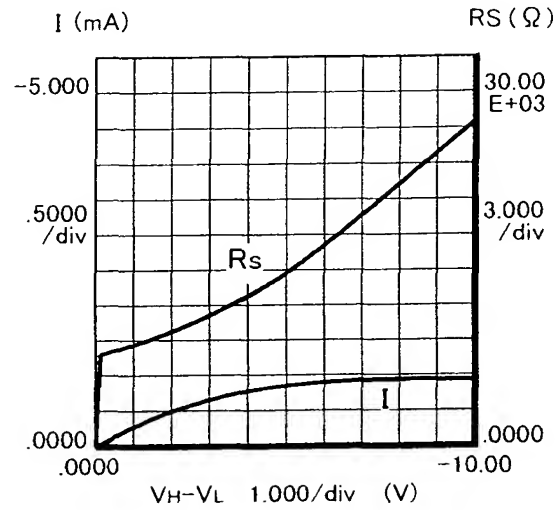


FIG.9(B)

R=0.2

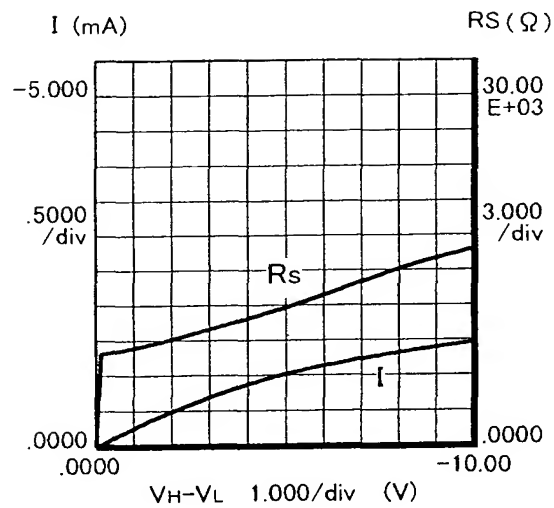
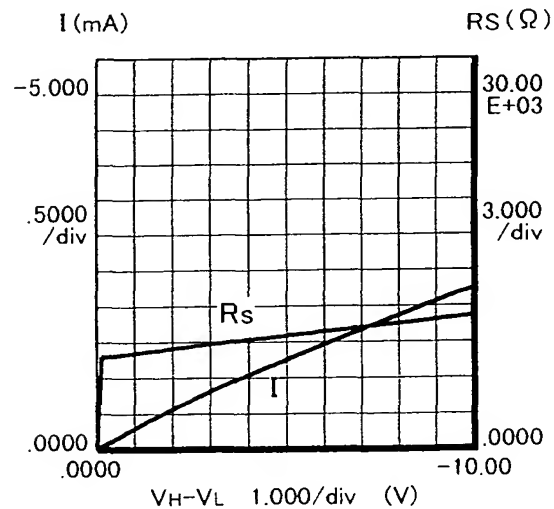


FIG.9(C)

R=0.4





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FIG.10(A)

R=0.5

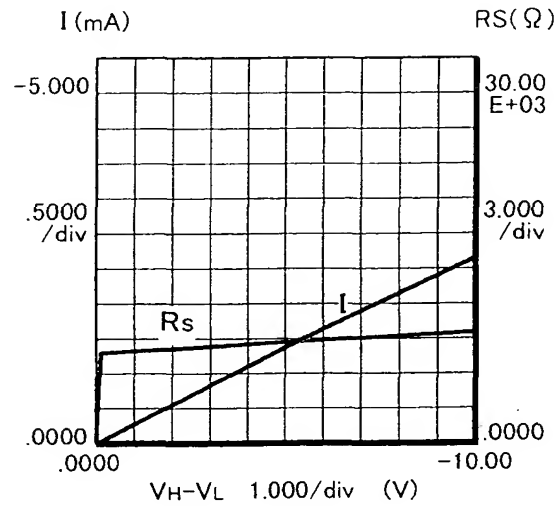


FIG.10(B)

R=0.6

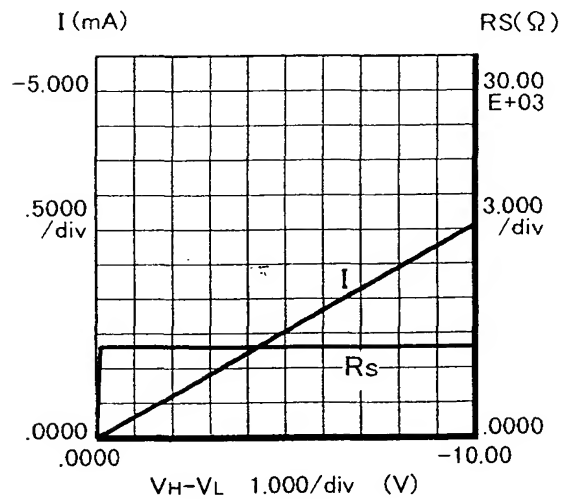


FIG.10(C)

R=0.8

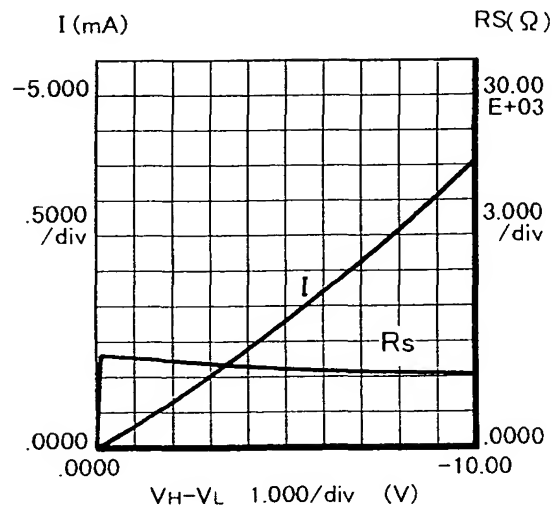


Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 50 with a well region NW. A thin layer 52 is formed on the surface, with a P- region in the center and P+ regions on either side. The P+ regions are labeled 53 and 54. The entire structure is covered by a protective layer 51.

FIG.12